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AN44

Application Note

USING THE CDBCAPTURE SYSTEM WITH EMBEDDED A/D CONVERTERS

by

John Lis

INTRODUCTION

The CDBCAPTURE system can be used to collect data from embedded Analog to Digital Converters (ADCs). Thus system performance of the analog front end can be measured, analyzed and quantified. By analyzing the measured performance, noise sources can be identified, isolated, and corrective actions taken. Here CDBCAPTURE is used as an engineering tool, reducing development time during system test and integration. Another application could be using CDBCAPTURE in production for testing finished products and verifying system performance.

CDBCAPTURE

The CAPTURE interface board is a development tool that interfaces a Crystal Semiconductor ADC to a PC compatible computer. Digital data from the ADC is collected in a high speed digital FIFO, then transmitted to the PC over a serial COM port. Evaluation software is included to analyze the data and demonstrate the ADC's performance. The entire system consists of a CAPTURE interface board, serial cable, RS232 cable, and software.

The software included with the CDBCAPTURE system quantifies static and dynamic performance of ADC systems. Static testing includes Histogramming and calculation of the mean, standard deviation and variance. Dynamic testing includes Fast Fourier Transforms and analysis of the power spectrum. Here Signal to Noise Ratio (SNR), Signal to Noise plus Distortion (SINAD), Signal to Distortion Ratio (SDR), and Signal to Peak Noise (SPN) figures are calculated. Time domain plots are available to visualize signals in the time domain and confirm operation.

CDBCAPTURE WITH EMBEDDED ADCs

The CDBCAPTURE circuit board is designed to directly interface with most Crystal Semiconductor ADC evaluation boards. This permits a quick and easy method to quantify and verify the ADC's performance. However, it is often desirable to measure the ADC's performance in the actual system or to measure the overall system performance. To collect data from an embedded ADC, a special serial cable needs to be designed. This cable incorporates the digital interface circuitry which exists on the evaluation board. This cable is connected to the appropriate signals on the ADC.

To collect data from an embedded ADC, the digital interface circuitry on the evaluation board needs to be incorporated on a modified serial

Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445-7222 FAX 445-7581
http://www.crystal.com

cable. Figure 1 is a block diagram illustrating the process. On the top of Figure 1, the evaluation board CDBXXXX contains digital interface circuitry which translates signals from the ADC to three standard serial signals named FRAME, SCLK and SDATA. The timing and format of these signals vary from device type to device type.

In an embedded ADC application, the digital interface circuit, between the ADC and the CDBCPATURE circuit card, should be implemented on a small card attached to the serial cable as shown at the bottom of Figure 1. The appropriate digital input signals need to be identified. A method to connect to these signals from the embedded system to the cable is then implemented. The connection scheme varies for each application and is easy to implement.

The schematic for the digital interface circuitry is provided with the evaluation board data sheet. Locate the serial interface connector containing the signals: +5 V, GND, FRAME, SCLK, and SDATA on the schematic. Working from this connector, back to the ADC, identify the circuitry required to create the serial signals. This circuitry is implemented on a separate circuit board, attached to a 10 conductor ribbon cable with an IDC socket for its CDBCAPTURE interface. The ADC interface can be any connector scheme that is easy to implement. Possible alternatives include stake headers, test clips, circular connectors, or "D" style connectors.

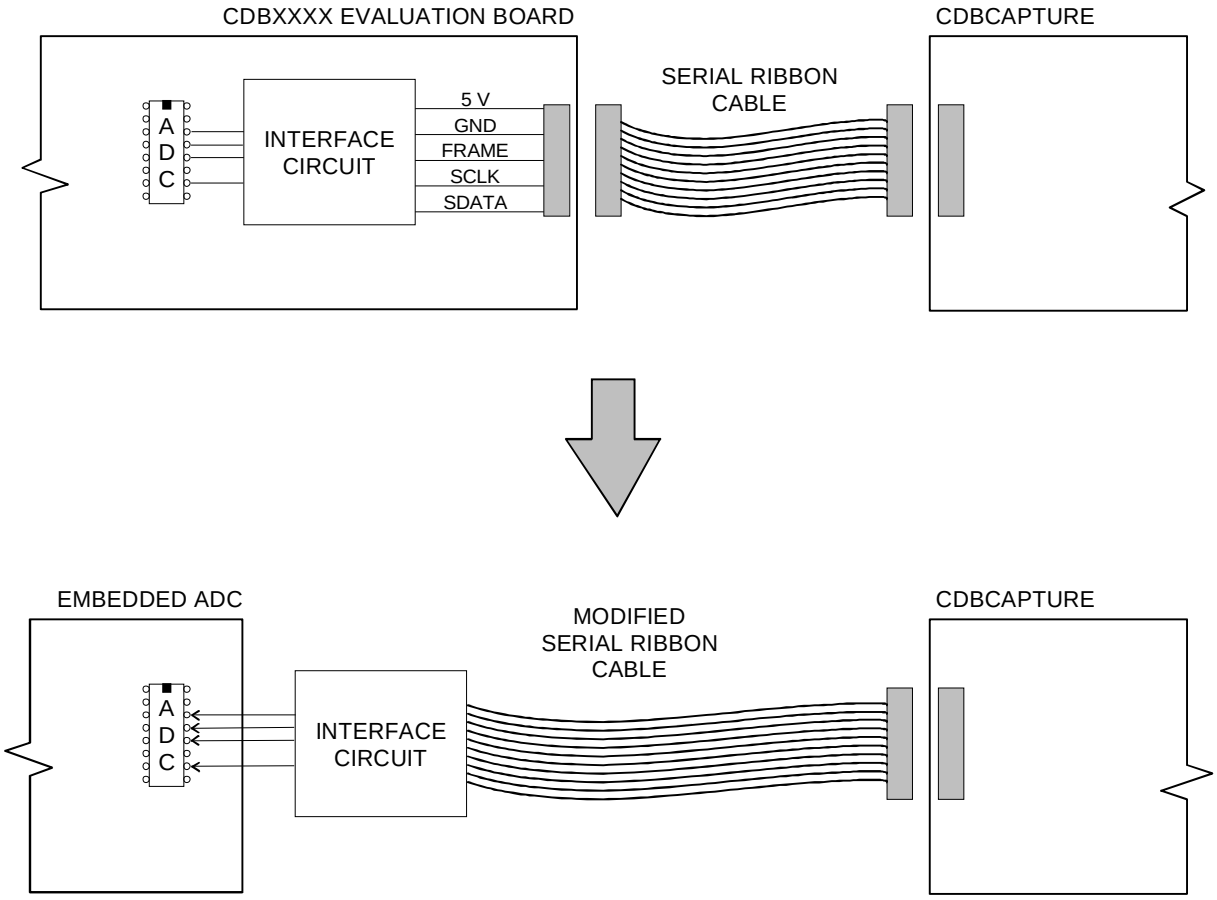

Figure 1. CDBCAPTURE INTERFACE

CS5508 EXAMPLE

The following example uses a CS5508 to illustrate the process of designing a modified serial cable. By examining the schematic for the CDB5508 evaluation board, the digital interface circuitry is identified. The schematic for the CDB5508 evaluation board is provided in Figure 1 of the CDB5505/6/7/8 data sheet. The digital interface portion is shown in Figure 2 below. Resistors R23, R24 and R25 are not required if the $\overline{CS}$ is always active. Also, U3B is always active when using the CAPTURE board, thus it can be changed to a general purpose buffer such as U2.

Figure 3 shows the schematic for the modified cable derived from Figure 2. The $\overline{DRDY}$, SCLK and SDATA signals are buffered to create the serial cable signals for the CAPTURE board. Five volt power is obtained from the embedded system and filtered by R1 and C1 before it is provided to the CAPTURE board. C2 is a bypass capacitor for U1.

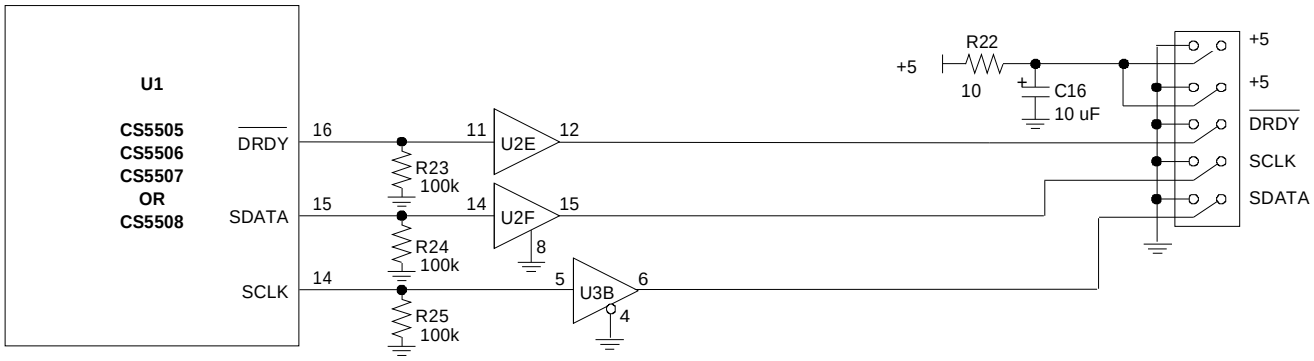

Figure 2. CDB5508 Evaluation Board Schematic for the Digital Interface

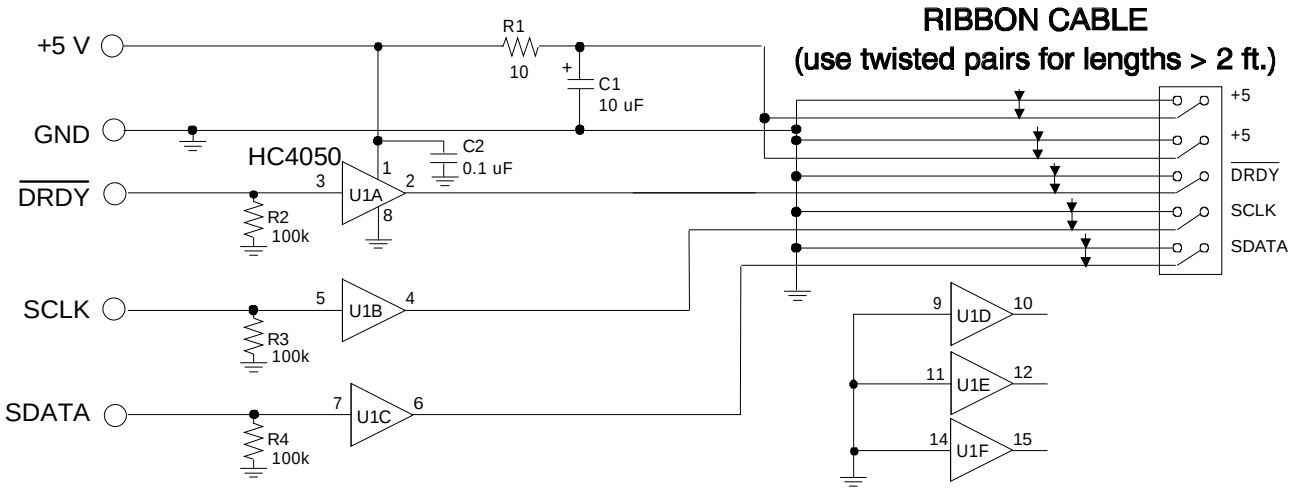

Figure 3. Modified Serial Cable Implementation of the Digital Interface

Figure 4 shows how the hardware can be implemented. The digital interface circuitry is built upon a small circuit board. A ribbon cable with a 10 circuit IDC socket is used for the CDBCAPTURE interface. Separate ground wires should be used for each signal return, and twisted pair ribbon cable used for lengths greater than two feet. The embedded interface uses color coded test clips. The test clips provide a means of interfacing an ADC without any special connectors designed in the system. However this method requires a little more setup time, since the appropriate signals need to be located on the circuit board.

CS5102A EXAMPLE

The CS5102A is used in the second example of an embedded application. The methodology for the cable design is the same as that in the first example using the CS5508. The digital interface circuitry is obtained from the CDB5101A/5102A evaluation board data sheet. This information is contained in the evaluation board's data sheet

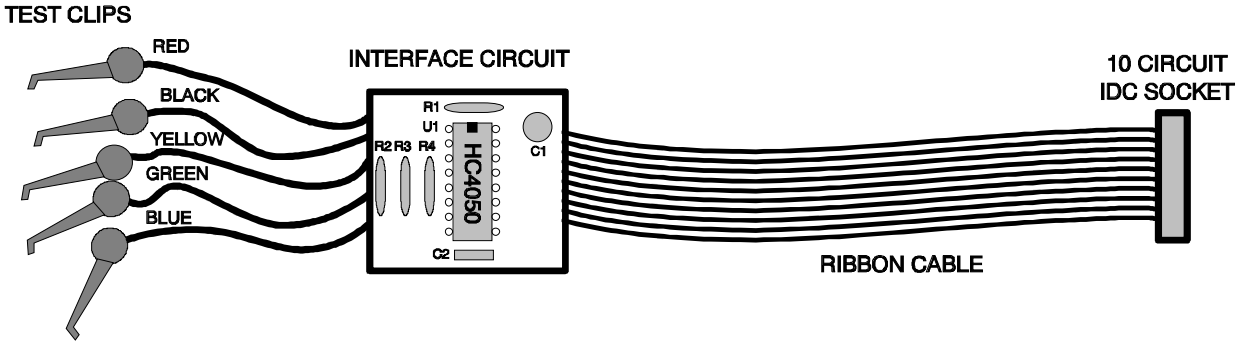

Figure 4. Construction of the Modified Serial Cable

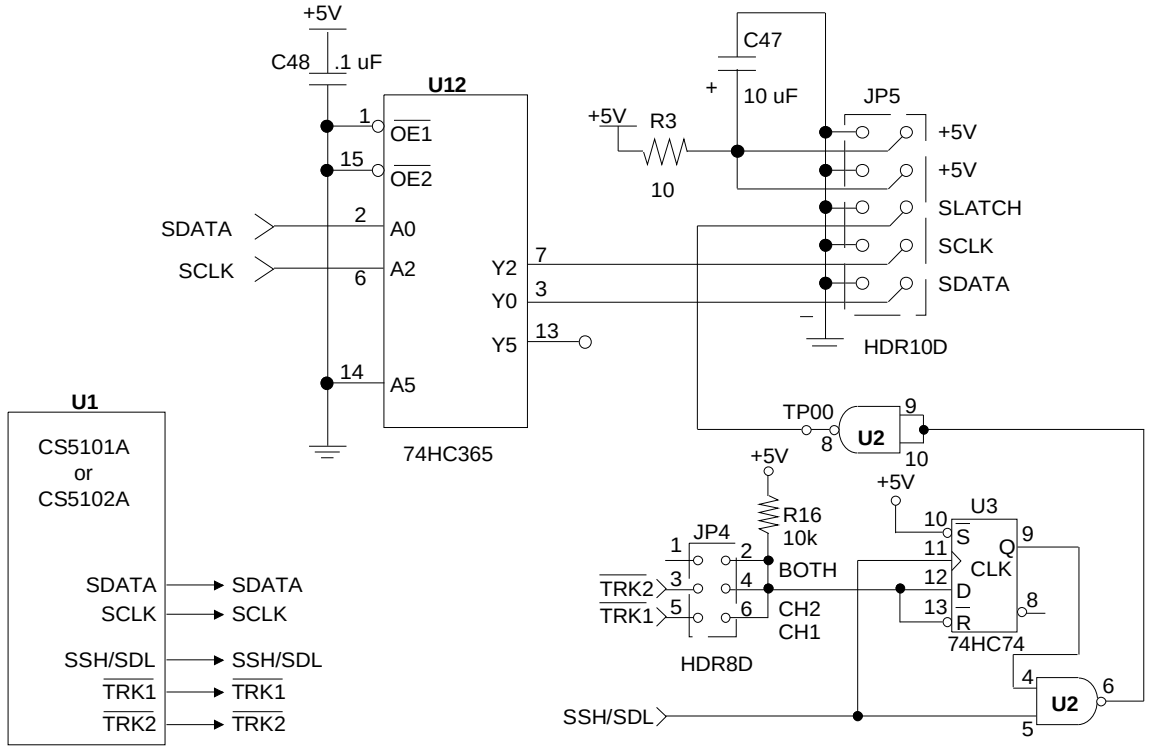

Figure 5. CDB5102A Evaluation Board Schematic for the Digital Interface

Figures 4, 5 and 6. The digital interface circuitry for the CS5102A is show in Figure 5.

Figure 6 is the way the digital circuitry is implemented on the modified serial cable.

Figure 7 is the hardware implementation of the modified serial cable shown in Figure 6. In this example, the embedded system is designed with a test connector. The modified serial cable is built with a connector which mates to the system test connector. The test connector provides a convenient and reliable means of interfacing the ADC.

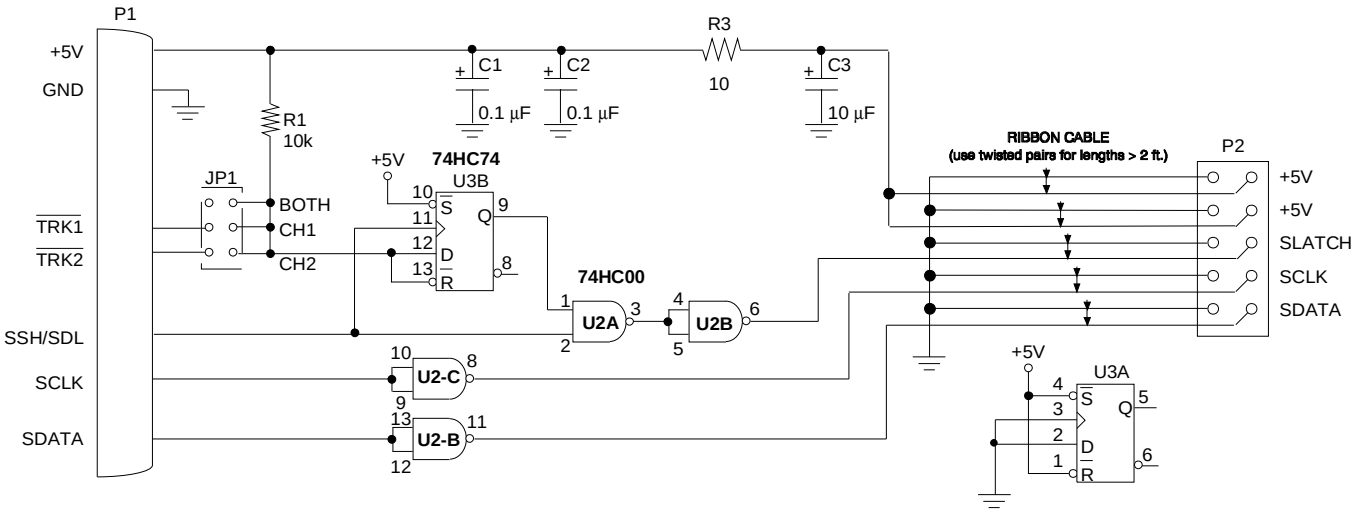

Figure 6. Modified Serial Cable Implementation of the Digital Interface

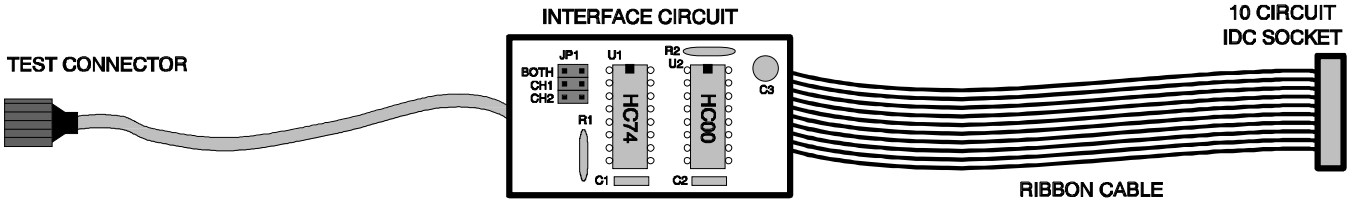

Figure 7. Construction of the Modified Serial Cable

Testing An Embedded ADC

System performance can be measured by interfacing the embedded ADC. The previous sections described the hardware modification required to interface a Crystal Semiconductor ADC with the CAPTURE board. Figures 8, 9, and 10 are the results of using the histogram test on a CS5101A in an embedded system.

Figure 8 is a histogram of a CS5101A operating in the bipolar mode with the analog input pin grounded right at the package. Data book performance is expected, if proper design practices have been used in developing the circuit and layout. In Figure 8, the mean is -0.69 counts, which is well within the typical specification of two counts for the bipolar offset. The standard deviation is 0.49 counts. This translates to 67 uV$_{RMS}$ (0.49 *x* 9 *volts*/2^{16}). The CS5101A data sheet specifies 70 uV$_{RMS}$ typical.

A buffer op-amp is integrated in the system and a data set is collected and displayed in Figure 9. Both the mean and standard deviation numbers changed with the addition of the op-amp. The op-amp added 0.66 counts to the offset or 91 *u*V. The RMS noise increased to 0.63 counts or 87 *u*V.

Figure 10 shows the histogram for the ADC, buffer op-amp, and signal source. The signal source output is set at zero volts. The histogram statistics indicate an offset of 1.59 counts or 218 *u*V and the RMS noise is at 218 *u*V. Note, that as more components are added to the system, the offset changes and the noise increases. These changes can be used to isolate and identify problems.

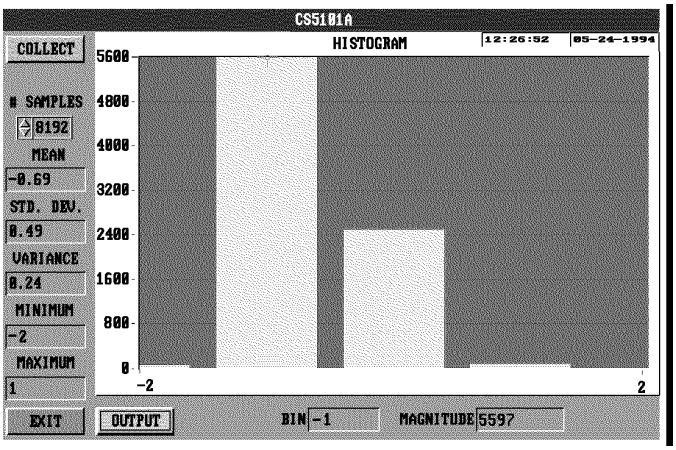

Figure 8. Histogram of a CS5101A with the Input Grounded

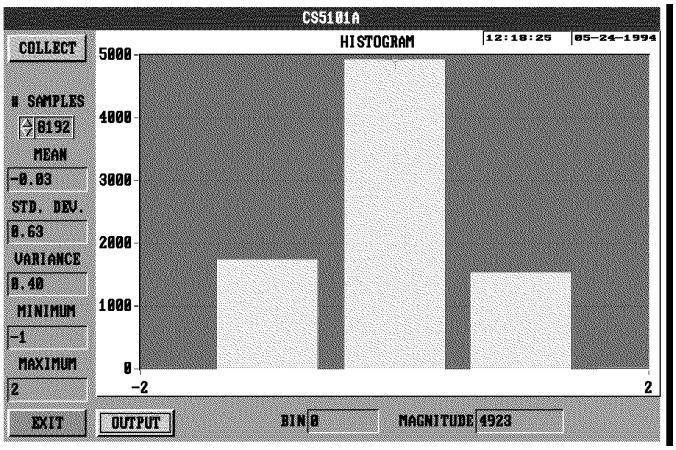

Figure 9. Histogram of a CS5101A with a Buffer Op-Amp

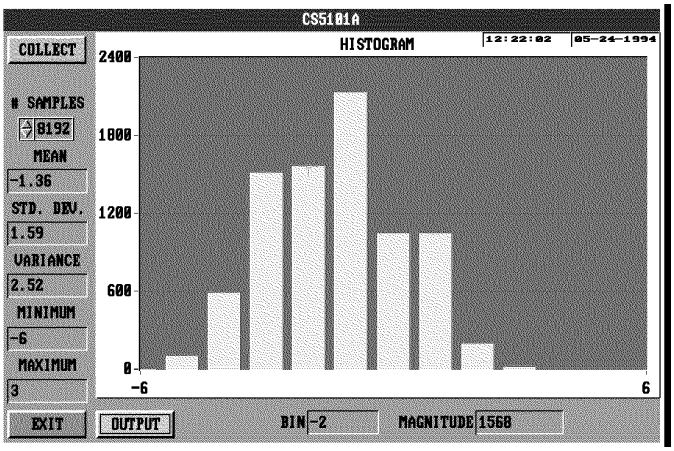

Figure 10. Histogram of a CS5101A with a Signal Source

CONCLUSION

The CDBCAPTURE system is designed to easily connect to most Crystal Semiconductor ADC evaluation boards. Digital circuitry is included on the evaluation boards to implement a standard serial data bus. The CAPTURE board is software reconfigurable to adjust for different ADCs and future products. The CDBCAPTURE system permits easy transfer of digital data to a PC for analysis.

Many times it is desirable to collect data from the ADC while it is operating inside a complete acquisition system. In this case, the digital interface circuitry for the CAPTURE board is implemented outside the system on a modified cable. The electrical system has to provide the appropriate interconnect scheme, using either connectors or test points to clip onto.

The modified serial cable allows the user to measure performance of the ADC while it is embedded in an electrical system. The ADC as well as the system performance can be measured and quantified. This information is used to isolate problems and investigate how certain subsystems interact with each other.

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